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Methods Of Forming Non-Volatile Resistance Variable Devices And Methods Of Forming Silver Selenide Comprising Structures

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INVENTORS:

Terry L. Gilton
Kristy A. Campbell
John T. Moore

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TECHNICAL FIELD

This invention relates to methods of forming non-volatile resistance variable devices, and to methods of forming silver selenide comprising structures.

BACKGROUND OF THE INVENTION

Semiconductor fabrication continues to strive to make individual electronic components smaller and smaller, resulting in ever denser integrated circuitry. One type of integrated circuitry comprises memory circuitry where information is stored in the form of binary data. The circuitry can be fabricated such that the data is volatile or non-volatile. Volatile storing memory devices result in loss of data when power is interrupted. Non-volatile memory circuitry retains the stored data even when power is interrupted.

This invention was principally motivated in making improvements to the design and operation of memory circuitry disclosed in U.S. Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796 to Kozicki et al., which ultimately resulted from U.S. Patent Application Serial No. 08/652,706, filed on May 30, 1996, disclosing what is referred to as a programmable metallization cell. Such a cell includes opposing electrodes having an insulating dielectric material received therebetween. Received within the dielectric material is a

variable resistance material. The resistance of such material can be changed between low resistance and high resistance states. In its normal high resistance state, to perform a write operation, a voltage potential is applied to a certain one of the electrodes, with the other of the electrode being held at zero voltage or ground. The electrode having the voltage applied thereto functions as an anode, while the electrode held at zero or ground functions as a cathode. The nature of the resistance variable material is such that it undergoes a change at a certain applied voltage. With such voltage applied, a low resistance state is induced into the material such that electrical conduction can occur between the top and bottom electrodes.

Once this occurs, the low resistance state is retained when the voltage potentials are removed. Such can effectively result in the resistance of the mass of resistance variable material between the electrodes dropping by a factor of 1,000. Such material can be returned to its highly resistive state by reversing the voltage potential between the anode and cathode. Again, the highly resistive state is maintained once the reverse voltage potentials are removed. Accordingly, such a device can, for example, function as a programmable memory cell of memory circuitry.

The preferred resistance variable material received between the electrodes typically and preferably comprises a chalcogenide material having metal ions diffused therein. One specific example includes one or more layers of germanium selenide having silver ions diffused therein and one or more layers

of silver selenide having excess silver ions diffused therein. It is, however, difficult to form silver rich silver selenide.

While the invention was principally motivated in addressing the above issues, it is in no way so limited. The artisan will appreciate applicability of the invention in other aspects unrelated to the above issues, with the invention only being limited by the accompanying claims as literally worded without limiting reference to the specification, and as appropriately interpreted in accordance with the doctrine of equivalents.

SUMMARY

The invention includes methods of forming non-volatile resistance variable devices, and methods of forming silver selenide comprising structures. In one implementation, a method of forming a non-volatile resistance variable device includes forming a patterned mass comprising elemental silver over a substrate. A layer comprising elemental selenium is formed over the substrate and including the patterned mass comprising elemental silver. The substrate is exposed to conditions effective to react only some of the elemental selenium with the elemental silver to form the patterned mass to comprise silver selenide. Unreacted elemental selenium is removed from the substrate. A first conductive electrode is provided in electrical connection with one portion of the patterned mass comprising silver selenide. A germanium selenide comprising material is provided in electrical connection with another portion of the patterned mass comprising silver selenide. A second conductive electrode is provided in electrical connection with the germanium selenide comprising material.

In one implementation, a method of forming a silver selenide comprising structure includes forming a substrate comprising a first outer portion and a second outer portion. The first outer portion comprises a patterned mass comprising elemental silver. The second outer portion does not comprise elemental silver. A layer comprising elemental selenium is formed over the first and second outer portions. The substrate is exposed to oxidizing conditions effective to both, a) react elemental selenium received over the first portion with elemental silver to form the patterned mass to comprise silver selenide,

and b) remove elemental selenium of the layer over the second outer portion from the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic perspective view of a semiconductor wafer fragment/section in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is an alternate view of the Fig. 3 wafer fragment at an alternate processing step subsequent to that shown by Fig. 3.

Fig. 6 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 7 is a view of the Fig. 6 wafer fragment at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is an alternate view of the Fig. 3 wafer fragment at an alternate processing step subsequent to that shown by Fig. 3.

Fig. 9 is a diagrammatic perspective view of an alternate embodiment semiconductor wafer fragment/section in process in accordance with an aspect of the invention.

Fig. 10 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that shown by Fig. 9.

Fig. 11 is a view of the Fig. 10 wafer fragment at a processing step subsequent to that shown by Fig. 10.

Fig. 12 is a diagrammatic perspective view of another alternate embodiment semiconductor wafer fragment/section in process in accordance with an aspect of the invention.

Fig. 13 is a view of the Fig. 12 wafer fragment at a processing step subsequent to that shown by Fig. 12.

Fig. 14 is a view of the Fig. 13 wafer fragment at a processing step subsequent to that shown by Fig. 13.

Fig. 15 is a view of the Fig. 14 wafer fragment at a processing step subsequent to that shown by Fig. 14.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Exemplary embodiment methods of forming a non-volatile resistance variable device are initially described with reference to Figs. 1 - 8. Fig. 1 depicts a substrate fragment 10 comprising a base substrate 12 and a first conductive electrode material 14 formed thereover. Base substrate 12 might comprise any suitable supporting substrate, for example a semiconductor substrate which includes bulk monocrystalline silicon. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Also in the context of this document, the term "layer" encompasses both the singular and the plural unless otherwise indicated. Exemplary preferred material for layer 14 is elemental tungsten.

An insulative material 16 is formed over first conductive electrode material 14. Such has been patterned by any suitable patterning method (i.e., lithography, such as photolithography) to form an opening 18 therethrough to

first conductive electrode material 14. Opening 18 comprises some desired shape of at least a portion of a final resistance setable structure of the device being fabricated, as will be apparent from the continuing discussion.

Referring to Fig. 2, opening 18 has been filled with an elemental silver comprising material 20 in electrical connection with first conductive electrode material 14. An exemplary preferred material for material 20 includes at least 50 molar percent elemental silver, even more preferably at least 95 molar percent elemental silver, and even more preferably greater than 99 molar percent elemental silver. In the illustrated preferred example, insulative material 16 has a substantially planar outermost surface proximate opening 18, and patterned mass/elemental silver comprising material 20 within opening 18 has an outermost surface which is co-planar with the insulative material outer surface. Further, patterned mass 20 can be considered as having some maximum first thickness, with an example thickness range being from about 50 Angstroms to about 2000 Angstroms.

One example method of producing the construction illustrated by Fig. 2 would be to deposit a layer of silver comprising material blanketly over the substrate, and then planarizing such layer back at least to the top of outer insulative layer 16. By way of example only, such deposition might occur by chemical or physical means. Further, the polishing or planarizing could occur by resist etch back, chemical polishing, mechanical polishing or any combination thereof, or by any other existing or yet-to-be-developed method. Further, alternately and by way of example only, the illustrated Fig. 2 construction might

be fabricated by an electroless or other deposition of silver comprising material 20 within the illustrated opening such that material 20 effectively only deposits therein and grows upwardly, with the growth preferably being stopped where material 20 approximately reaches the upper surface of insulative material 16. Regardless, Fig. 2 depicts but one example of forming a patterned mass comprising elemental silver over a substrate.

Referring to Fig. 3, a layer 22 comprising elemental selenium is formed over substrate 10 and including patterned mass 20 comprising elemental silver. Preferably, layer 22 comprises elemental selenium of at least 90 molar percent, more preferably at least 95 molar percent elemental selenium, and even more preferably greater than 99 molar percent elemental selenium.

Referring to Fig. 4, substrate 10 has been exposed to conditions effective to react elemental selenium 22 received over the elemental silver of mass 20 to form at least a portion of the filled opening/patterned mass to comprise silver selenide 25. In the depicted and preferred embodiment, such exposing to the conditions are effective to react only some of elemental selenium comprising layer 22, with those portions formed over insulative material 16 being essentially unreacted. In the Fig. 4 depicted and preferred embodiment, the exposing is illustrated as forming the patterned mass to entirely comprise silver selenide material 25. Regardless, the exposing preferably forms that portion of the patterned mass which is transformed to comprise at least 50 molar percent silver selenide, and more preferably at least 80 molar percent silver selenide.

Further preferably, that portion which is formed is ideally substantially homogenous.

Fig. 5 depicts an alternate embodiment 10a. Like numerals from the first embodiment are utilized where appropriate, with differences being indicated by the suffix "a". Fig. 5 depicts forming an outermost portion 25a of the patterned mass to comprise silver selenide, while an innermost portion 20a of the patterned mass remains as the deposited silver comprising material initially formed. By way of example only, the remaining thickness of innermost portion 20a is preferably from 0 to 10 percent of the total thickness of the illustrated patterned mass. Each of Figs. 4 and 5 depicts but one embodiment wherein the exposing forms more than one-half of the filled opening to comprise silver selenide. Alternately, by way of example only, one-half or less than one-half might be filled. Further in the preferred embodiment as shown, the exposing forms the patterned mass to have a maximum second thickness which is greater than the maximum first thickness.

One example preferred process for the subject exposing includes annealing the substrate at a temperature of from about 40°C to about 100°C at a pressure of from about 30 mTorr to 760 Torr for from about one to three hours. Higher temperatures typically result in a higher annealing rate. Conditions and time can be controlled to achieve a desired amount of the mass to be transformed to silver selenide comprising material. Further, by way of example only, annealing in a suitable oxidizing atmosphere is also a possibility, as is more fully described below.

Referring to Fig. 6, unreacted elemental selenium 22 has been removed from the substrate. The preferred removing, as shown, removes all remaining unreacted elemental selenium from the substrate. One example of removing comprises chemical etching, and preferably in a manner which is selective to remove elemental selenium comprising material 16 selectively relative to silver selenide comprising material 25. An example wet etch for doing so would include utilizing hydrogen peroxide, for example at from room temperature to 50°C and ambient pressure. An example dry process would include plasma etching using CF_4. Further by way of example only, an alternate process for removing unreacted elemental selenium comprises increasing the temperature of the substrate to closer to the melting temperature of selenium, say from 200°C to 250°C, and at atmospheric pressure for from 10 minutes to one hour, effective to cause evaporation of the unreacted selenium from the substrate.

Referring to Fig. 7, a germanium selenide material layer 26 (i.e., preferably 40 molar percent germanium and 60 molar percent selenium) is formed over and in electrical connection with silver selenide comprising material 25. A second conductive electrode material 28 is formed thereover, and thereby in electrical connection with silver selenide 25 through material 26. Second conductive electrode material 28 might be the same as first conductive electrode material 14, or be different. An exemplary preferred material for electrode 28 in the depicted and described embodiment is elemental silver. Regardless, in the preferred embodiment such provides exemplary processing of providing a first conductive electrode in electrical connection with one portion of

patterned mass 25 comprising silver selenide, providing a germanium selenide comprising material in electrical connection with another portion of the patterned mass comprising silver selenide, and providing a second conductive electrode in electrical connection with the germanium selenide comprising material.

The above-described exemplary preferred embodiment processes conducted the exposing and the removing in different or separate processing steps. The invention also contemplates conducting the exposing and the removing in the same or single common processing step. Fig. 8 depicts an alternate embodiment 10c which depicts an alternate processing of the Fig. 3 wafer which produces a slightly modified construction to that depicted by Fig. 4. In Fig. 8, the exposing and the removing have occurred in a common processing step comprising at least 100°C and an atmosphere which removes unreacted elemental selenium by oxidation thereof. Preferably, the oxidizing atmosphere utilizes a weak oxidizer or a dilute oxidizer, for example at less than or equal to five percent by volume oxidizer, with less than or equal to one percent being more preferred. An example preferred oxidizing atmosphere comprises at least one of N_2O, NO_x, O_3, F_2 and Cl_2. By way of example only, preferred conditions include an elevated temperature of from 40°C to 250°C, a pressure at from 30 mTorr to 760 Torr and from 30 minutes to two hours.

The oxidizing conditions and atmosphere are preferably selected to be sufficiently dilute or weak, as identified above, to prevent the complete oxidation of selenium comprising material 22 over patterned mass 20 prior to driving (either physically or by reacting) elemental selenium into patterned mass 20 such

that an effective silver selenide mass 25c is formed. However, such oxidizing will typically result in some removal of elemental selenium by oxidation at the outermost portion of elemental selenium comprising layer 22 over the patterned mass during the oxidizing. Most preferably in this and any embodiment, the exposing drives at least a majority of that portion of the elemental selenium received over the patterned mass into the patterned mass.

The invention further contemplates a method of forming any silver selenide comprising structure regardless of whether such is utilized in the fabrication of a non-volatile resistance variable device. Such method contemplates forming a substrate comprising a first outer portion and a second outer portion, with the first outer portion constituting a patterned mass comprising elemental silver and the second portion not comprising elemental silver. By way of example only and with respect to Figs. 2 and 3, an outermost portion of patterned mass 20 comprising elemental silver comprises an exemplary first outer portion, with the outermost portion of insulative 16 constituting an exemplary second outer portion. A layer comprising elemental selenium is formed over the first and second outer portions. The substrate is exposed to oxidizing conditions, by way of example only such as those described above, effective to both a) react elemental selenium received over the first portion with elemental silver to form the patterned mass to comprise silver selenide, and b) remove elemental selenium of a layer over the second outer portion from the substrate. Preferably, the exposing removes all unreacted elemental selenium from the substrate. Further, and in accordance with the above-described preferred embodiment, such exposing

will tend to remove some of the elemental selenium of the layer over the first portion from the substrate, but still preferably drive at least a majority of that portion of the elemental selenium received over the first portion into the patterned mass, and more preferably at least 80 molar percent. Further, such exposing preferably forms the patterned mass to have a maximum second thickness which is greater than its maximum first thickness immediately prior to the exposing.

The depicted and above-described embodiments show processes wherein at least a majority and in one case essentially all of the material within opening 18 is formed to comprise elemental silver. Figs. 9 - 11 illustrate an alternate embodiment 10d. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by the suffix "d" or with different numerals. Fig. 9 depicts an alternate elemental silver comprising material 20d received within opening 18. Such comprises a lower exemplary germanium selenide portion 21 (i.e., preferably 40 percent germanium and 60 percent selenium), and an overlying preferred 99 percent-plus pure elemental silver region 23. By way of example only, such could be formed by suitable deposition and planarization relative to insulative layer 16. A selenium comprising layer 22d is formed thereover.

Referring to Fig. 10, substrate 10d has been subjected to the preferred exposing and removing processing (either together or in different steps) effective to form a silver selenide mass 25d and to remove at least some, and preferably all, unreacted elemental selenium from the substrate.

Referring to Fig. 11, another germanium selenide layer 26d and a second electrode 28d are formed thereover.

The above-described embodiments describe and depict exemplary methods of forming a patterned mass comprising elemental silver. Such embodiments depict forming a patterned opening within insulative material over a substrate, and at least partially filling the opening with an elemental silver comprising material. However, the invention contemplates any method of forming a patterned mass comprising elemental silver. By way of example only, one such alternate process is described with reference to Figs. 12 - 15.

Fig. 12 depicts another alternate embodiment 10e, with like numerals from the first embodiment being utilized and differences being indicated with the suffix "e" or with different numerals. Fig. 12 depicts the depositing of a silver comprising material 20e. Material 20e has been patterned, for example by photopatterning and then subtractively etching after the patterning. Other patterning, such as laser patterning or any other method of patterning, is contemplated, whether existing or yet-to-be-developed.

Referring to Fig. 13, an elemental selenium comprising layer 22e is formed over patterned mass 20e.

Referring to Fig. 14, the substrate has been exposed to conditions effective to react only some of elemental selenium 22e with the elemental silver to form a patterned mass 25e to comprise silver selenide. Any of the above-described processing, including an oxidation process which removes 22e from

the process during the exposing, is contemplated, of course, and are only preferred examples.

Referring to Fig. 15, a preferred germanium selenide layer 26e and a preferred second electrode 28e are formed thereover.

The above constructions can be effectively preferably fabricated to form programmable metallization cells over memory and other integrated circuitry.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.